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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,906	12/30/2003	Jong-Cheol Lee	8836-223 (ID12244-US)	7419
22150	7590	07/10/2007	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			SIDDIQUI, SAQIB JAVAID	
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/748,906	Applicant(s) LEE ET AL.	
	Examiner Saqib J. Siddiqui	Art Unit 2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3 and 5-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3 and 5-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicant's response was received and entered May 02, 2007.

- Claims 1, 3, 5, 8, 11, 14 and 17-18 have been amended.
- Claims 2 and 4 have been canceled.
- Claims 1, 3, and 5-18 are pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-18 filed May 02, 2007 have been considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

The Applicant contends that prior art of record Porter et al. does not teach a first path circuit receiving a first data single rate signal and a first and second transmission signal pair. The Examiner respectfully disagrees.

The Examiner would like to respectfully direct Applicant's attention towards "In single data rate operation, the second piece of data is the same as the first piece of data and the second piece of data represents the same memory address or location as the first piece of data. The data selected by the odd path 204 or the even path 205 is passed to the output register 102 and the holding register 103 substantially simultaneously. The data is passed on the rising edge of the clock, but there may be a small delay in passing the data to the holding register 103." (column 5, lines 20-30)

"A number of data lines may be presented to each mux. A list of possible data lines are: multiple data bits (if the internal data path is wider than necessary), redundant data, and buffered write data. Which data line is selected is determined by peripheral

logic. Each data mux provides the correct data (the even mux 305 provides EVEN DATA and the odd mux 304 provides ODD DATA)." (column 6, lines 5-15).

Further, looking at Figure 3A the data unit 101 provides the path with a first and second single data rate signal and the transmission signal pairs are PASSE PASSO and PASSEd and PASSOd. Using these signals the buffers produce a first and second output signal. Therefore, the prior art of reference teaches the limitations as recited in claims 1, 3 and 5-18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 3, 14 & 17-18 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Porter et al. (Porter hereinafter) US Pat no. 6,516,363 B1.

As per claim 1:

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Porter teaches a semiconductor memory device operable in a merged data input/output pin (DQ) test mode, comprising: a first path circuit (Figure 2 # 204) receiving a first data bit, a first single data rate signal and a first transmission signal pair and producing a first path output signal (Figure 3A, columns 5-6); a second path circuit (Figure 2 # 205) receiving a second data bit, a second single data rate signal and a second transmission signal pair and producing a second path output signal (Figure 3A, columns 5-6); and a merged output generator (Figure 2 # 102) configured to generate a merged data bit based on the first path output signal and the second path output signal having a single data rate (SDR) pattern and/or a dual data rate (DDR) pattern as determined by the first and second single data rate signals and the first and second transmission signal pairs (Figure 2 # 102, column 2, lines 10-16).

As per claim 3:

Porter teaches the semiconductor memory device as rejected in claim 1 above, further comprising a control signal generator configured to generate a first and second SDR signal and a first and second transmission signal pair (Figure 3A # 101).

As per claim 14:

Porter teaches the semiconductor memory device as rejected in claim 1 above, wherein the merged output generator comprises; a NAND gate receiving outputs of the first and second path circuits; and an inverter converting an output of the NAND gate into the merged data bit (Figure 3D).

As per claims 17-18:

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Claims 17-18 are directed to semiconductor of the device of claims 1-16. Porter teaches as stated above, the device as set forth in claims 1-16. Therefore, Porter also teaches as stated above, the semiconductor as set forth in claims 17-18.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5-13, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Porter US Pat no. 6,516,363 B1.

As per claims 5, 8 & 11:

Porter substantially teaches a semiconductor memory device operable in a merged data input/output pin (DQ) test mode, comprising: a first path circuit (Figure 2 # 204); a second path circuit (Figure 2 # 205); and a merged output generator (Figure 2 # 102) configured to generate a merged data bit having a single data rate (SDR) pattern and/or a dual data rate (DDR) pattern (column 2, lines 10-16).

Porter does not explicitly mention the exact elementary details of NOR, NAND gates and inverters. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the exact number of logic gates and inverters as specified in the application, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

As per claim 6:

Porter teaches the semiconductor memory device as rejected in claim 5 above, wherein the first SDR signal is generated in response to a main signal of the first transmission signal pair and a complementary signal of the second transmission signal pair (Figure 3A, "MUXE*" & "MUX0*").

As per claim 7:

Porter teaches the semiconductor memory device as rejected in claim 5 above, wherein the second SDR signal is generated in response to a complementary signal of the first transmission signal pair and a main signal of the second transmission signal pair (Figure 3A, "MUXE*" & "MUX0*").

As per claim 9:

Porter teaches the semiconductor memory device as rejected in claim 8 above, wherein the first data path circuit propagates the first data bit generated at a first edge of a clock signal (column 3, lines 15-50).

As per claim 10:

Porter teaches the semiconductor memory device as rejected in claim 8 above, wherein the first path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal (Figure 3A).

As per claim 12:

Porter teaches the semiconductor memory device as rejected in claim 11 above, wherein the second data path circuit propagates the first data bit generated at a second edge of a clock signal (column 3, lines 20-60).

As per claim 13:

Porter teaches the semiconductor memory device as rejected in claim 11 above, wherein the second path circuit further comprises an NMOS transistor resetting the output node of the transmission gate in response to a reset signal (Figure 3A).

As per claim 15:

Porter teaches the semiconductor memory device as rejected in claim 9 above, wherein the first edge is a rising edge of the clock signal (column 3, lines 5-60).

As per claim 16:

Porter teaches the semiconductor memory device as rejected in claim 12 above, wherein the second edge is a falling edge of the clock signal (column 3, lines 5-60).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

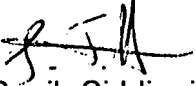
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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Saqib Siddiqui
Art Unit 2138
07/03/2007


GUY LAMARRE
PRIMARY EXAMINER